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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CERVETTI, DAVID GARCIA	
ART UNIT	PAPER NUMBER
2136	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,203	TOMOHIRO, ICHIRO	
	Examiner	Art Unit	
	David G. Cervetti	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending and have been examined.

2. Applicant's arguments filed May 18, 2005, have been fully considered but they are not persuasive.

Response to Amendment

3. Examiner approves the amendment to the specification. The objection to the specification is withdrawn.

4. Examiner approves the replacement sheet for figures 1 and 2 received on May 18, 2005. The objection to the drawings is withdrawn.

5. Examiner approves the amendment to the abstract of the disclosure. The objection to the abstract of the disclosure is withdrawn.

6. Applicant's remarks are based on language found in the specification, not on the claimed language. Examiner has given the claims the broadest reasonable interpretation consistent with the specification. Kasai et al.'s system provides a data control circuit (determination circuit) that generates a signal based on two values (readout value and security information).

7. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

8. Applicant's opinion that the present invention provides better data protection has been considered. Applicant's paragraph regarding why the present invention provides

better data protection provides a wealth of information regarding the differences between the Prior Art cited by Examiner and the present invention, but it is not part of the claims.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-3, 6, 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasai et al. (US Patent Number: 6,229,731).

Regarding claim 1, Kasai et al. teach a semiconductor storage device having a security function for imposing limitation on data rewriting (column 1, lined 18-28, column 3, lines 42-59), the semiconductor storage device comprising: at least one non-volatile memory cell array block which is capable of receiving concurrent electrical erasure (column 5, lines 25-37); at least one memory region, each one of said at least one memory region being provided in the at least one memory cell array block, for storing a security release key (column 1, lines 61-67, column 2, lines 1-10, column 5, lines 22-24); at least one non-volatile storage means for storing a security registration lock corresponding to each of the at least one memory cell array block (column 2, lines 32-50); a determination circuit for comparing a value which is generated based on the

security release key against a value which is generated based on the security registration lock to determine whether or not to grant release of the security function (column 2, lines 21-32, 56-67, column 3, lines 1-13); and a memory cell array data output switching circuit for, when an output signal from the determination circuit indicates a matching result of comparison (column 5, lines 38-52) between the value which is generated based on the security release key and the value which is generated based on the security registration lock, permitting data which is read from a corresponding one of the at least one memory cell array block to be externally output (column 5, lines 52-67, column 6, lines 1-3).

Regarding claim 2, Kasai et al. teach a semiconductor storage device according to claim 1, wherein: the semiconductor storage device further comprises at least one register for retaining an output signal output from the determination circuit (column 2, lines 32-50); and when an output signal output from the at least one register indicates that release of the security function is to be granted, the memory cell array data output switching circuit permits data which is read from a corresponding one of the at least one memory cell array block to be externally output.

Regarding claim 3, Kasai et al. teach a semiconductor storage device according to claim 1, further comprising instruction interpretation means (column 2, lines 57-67, column 3, lines 1-13) for interpreting an externally-input setting instruction to write at least one of the security release key and the security registration lock into the at least one memory region or the at least one non-volatile storage means, respectively.

Regarding claim 6, Kasai et al. teach a semiconductor storage device according to claim 1, which lacks means for reading the security release key and the security registration lock (column 3, lines 53-55).

Regarding claim 9, Kasai et al. teach a semiconductor storage device according to claim 1, further comprising a flag indicating that the security release key has been set (column 5, lines 29-33), wherein the flag is set automatically or manually after the security release key is written, thereby prohibiting additional writing to the corresponding one of the at least one memory cell array block.

Regarding claim 10, Kasai et al. teach a semiconductor storage device according to claim 1, wherein a wait operation is performed while writing the security release key to the at least one memory region (column 6, lines 11-35).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai et al. as applied to claim 2 above, and further in view of Matsuo et al. (US Patent Number: 5,974,513).

Kasai et al. teach the limitations as set forth under claim 2 above. However, Kasai et al. do not disclose expressly that a semiconductor storage device according to claim 2, wherein the determination circuit compares the value which is generated based on the security release key against the value which is generated based on the security registration lock for each of the at least one memory cell array block, and results of comparison are collaterally written in the at least one register.

Matsuo et al. teach a semiconductor storage device according to claim 2, wherein the determination circuit compares the value which is generated based on the security release key against the value which is generated based on the security registration lock (column 3, lines 45-53, column 4, lines 60-67, column 5, lines 1-50) for each of the at least one memory cell array block, and results of comparison are collaterally written in the at least one register.

Kasai et al. and Matsuo et al. are analogous art because they are from the same field of endeavor, semiconductor storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have a determination circuit to compare values and to store the result of the comparison to prevent data from being erased by mistake.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Matsuo et al. with the system of Kasai et al. for the benefit of semiconductor storage devices to obtain the invention as specified in claim 4.

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai et al. as applied to claim 1 above, and further in view of Arai (US Patent Number: 6,543,017).

Kasai et al. teach the limitations as set forth under claim 1 above. However, Kasai et al. do not disclose expressly a semiconductor storage device according to claim 1, further comprising a unidirectional conversion circuit or an encryption circuit, wherein results of converting the security release key and the security registration lock by means of the unidirectional conversion circuit or the encryption circuit are written to the at least one memory region and the at least one non-volatile storage means, respectively.

Arai teaches a semiconductor storage device according to claim 1, further comprising a unidirectional conversion circuit or an encryption circuit (column 3, lines 29-55, figure 1, reference character 102), wherein results of converting the security release key and the security registration lock by means of the unidirectional conversion circuit or the encryption circuit are written to the at least one memory region and the at least one non-volatile storage means, respectively (column 1, lines 33-43).

Kasai et al. and Arai are analogous art because they are from the same field of endeavor, semiconductor storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a conversion circuit or an encryption circuit to a semiconductor storage device to provide a secure processing environment in which confidential information can be securely processed.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Arai with the system of Kasai et al. for the benefit of semiconductor storage devices to obtain the invention as specified in claim 5.

14. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai et al. as applied to claim 1 above, and further in view of Araki et al. (US Patent Number: 5,374,847).

Regarding claim 7, Kasai et al. teach the limitations as set forth under claim 1 above. However, Kasai et al. do not disclose expressly a semiconductor storage device according to claim 1, wherein: the at least one non-volatile storage means is a one-time programmable ROM which prohibits rewriting and erasure; and rewriting and erasure are prohibited after the security registration lock is written.

Araki et al. teach a semiconductor storage device according to claim 1, wherein: the at least one non-volatile storage means is a one-time programmable ROM (column 7, lines 66-68, column 8, lines 1-6) which prohibits rewriting and erasure; and rewriting and erasure are prohibited after the security registration lock is written.

Kasai et al. and Araki et al. are analogous art because they are from the same field of endeavor, semiconductor storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use one-time programmable read only memory ("ROM") because it does not allow re-writing or erasure.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Araki et al. with the system of Kasai et al. for the benefit of semiconductor storage devices to obtain the invention as specified in claim 7.

Regarding claim 8, Kasai et al. teach the limitations as set forth under claim 1 above. Kasai et al. also teach a semiconductor storage device according to claim 1, wherein: the semiconductor storage device has a non-volatile lock function for locking the semiconductor storage device to prohibit rewriting and erasure after writing of the security registration lock has been performed (column 1, lines 12-30). However, Kasai et al. do not disclose expressly a semiconductor storage device according to claim 1, wherein: the at least one non-volatile storage means is a one-time programmable ROM which prohibits rewriting and erasure.

Araki et al. teach a semiconductor storage device according to claim 1, wherein: the at least one non-volatile storage means is a one-time programmable ROM which prohibits rewriting and erasure (column 7, lines 66-68, column 8, lines 1-6).

Kasai et al. and Araki et al. are analogous art because they are from the same field of endeavor, semiconductor storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use one-time programmable read only memory ("ROM") because it does not allow re-writing or erasure and to use a non-volatile lock function. Therefore, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Araki et al. with the system of Kasai et al. for the benefit of semiconductor storage devices to obtain the invention as specified in claim 8.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number: 5,708,715 to Vicard discloses an integrated circuit device with lock circuitry that controls operational enablement of a functional block.

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 7:00 am - 5:00 pm, off on Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DGC

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